CALL FOR APPLICATIONS – CHALLENGE: AI-NATIVE CHIP DESIGN

1. WHAT IS SPRIND?

SPRIND, the German Federal Agency for Breakthrough Innovation, identifies, funds, and scales groundbreaking innovations on behalf of the federal government. We fund teams directly, share the entrepreneurial risk, and support them operationally from concept to market.

Challenges and Funken are our main instruments for this. We define a specific problem; teams compete against one another and develop their solution over two to three stages. After each stage, a jury decides who advances. We guide the strongest teams all the way to market entry.

2. WHAT IS NADI?

The National Agency for Disruptive Innovation (NADI) is currently being established in the Netherlands. An independent institution designed to catalyze breakthrough innovation in areas of significant societal and economic importance, by absorbing the financial risk that the market is not yet ready to bear.

3. THE AI-NATIVE CHIP DESIGN CHALLENGE

Europe stands at a critical junction in its digital transformation. Artificial intelligence is rapidly advancing across every sector, from digital infrastructure and automotive to robotics, defense, and healthcare. At the same time, Europe remains heavily dependent on Asian and US players for advanced semiconductor chips. This dependency poses a direct threat to its technological sovereignty.

Yet supply chain vulnerability is only part of the problem. Chip development remains one of the most complex engineering endeavors in existence. Designing a single chip for cutting-edge Complementary Metal-Oxide-Semiconductor (CMOS) technology requires teams of a hundred or more specialists, with costs reaching deep into the hundreds of millions. These custom hardware solutions demand multi-year development cycles, whereas the AI models designed to run on them evolve in a matter of weeks. This massive mismatch stalls the entire innovation ecosystem.

At the same time, new opportunities are emerging. Moore's Law, the principle that computing power doubles roughly every two years while costs decrease, is hitting hard physical limits. As a result, the primary path for innovation is shifting toward architectural breakthroughs and radical efficiency gains. Meanwhile, advanced AI models and open-source technologies are lowering the barriers to entry.

It is precisely at this intersection of dependency and the urgent need for accelerated development that Europe has the opportunity for a strategic fresh start in semiconductors. AI holds the power to revolutionize chip design and build a new, native capacity for semiconductor engineering in Europe. By making AI the chip designer, development timelines can collapse from years to weeks. This will enable specialized, energy-efficient chip architectures for AI Gigafactories and core European industries, setting new benchmarks in performance and energy efficiency.

NADI and SPRIND are launching a joint Challenge to place Europe on an independent path in semiconductor development. By bringing together technical expertise, funding, and targeted networks, this initiative is built to overcome traditional chip design barriers and radically accelerate development cycles.

4. THE GOAL

The goal of the Challenge is to develop AI methods that enable the design of new chips within weeks. This development will directly lead to concrete, tape-out ready designs for high-performance chips.

Designed for speed and cost efficiency, the two-stage program spans an initial period of 20 months to provide targeted support for selected teams throughout their development. The overarching objective is to dramatically accelerate the chip design process. In addition, the Challenge aims to mobilize private venture capital and strategic investment, securing the financial resources required to build sustainable international competitiveness for European chip design innovations.

The initiative focuses primarily on CMOS-based chip architectures. However, to keep the search space open for new computing paradigms rather than restricting innovation to dominant architectures, photonic, neuromorphic, memristive, and analog computing concepts are also eligible to apply. Organoid computing platforms and quantum computing chips are explicitly excluded. Novel architectural concepts, such as in-memory computing, heterogeneous integration, or 3D stacking, are strongly encouraged.

SPRIND is dedicated to empowering innovators to realize breakthrough solutions. Following the completion of the second stage of this Challenge, SPRIND aims to provide outstanding teams with follow-on funding in the tens of millions of euros to enable the execution of their developed designs during the tape-out phase. Specific details regarding potential follow-on funding will be published at a later date.

The AI-Native Chip Design Challenge encourages radical solutions with transformative acceleration power. We are not looking for incremental improvements to existing methods and architectures, but true technological leaps.

FULL STACK APPROACH

This Challenge views chip design as a system-level problem. Hardware, software, and industrial application must align perfectly, as no single component can succeed in isolation.

An end-to-end stack is critical for success. Without a complete software stack, there is no developer engagement, no scalability, and no platform leverage. An integrated stack creates sustainable ecosystem momentum and fuels growth. Teams must therefore design the software stack right from the start, ensuring compatibility with existing environments by providing optimized Hardware Abstraction Layers.

This principle applies to both pillars of the Challenge. For chip development, the full-stack approach spans hardware, synthesis engines, runtime environments, and AI frameworks. For AI-driven design tools, it means covering the entire design pipeline—from specification and final layout to verification and downstream validation—rather than targeting isolated steps.

ECOSYSTEM

Chip design does not happen in isolation. It relies on tight feedback loops with manufacturing, packaging, EDA tools, material systems, and industrial end-use applications. A key driver for team success is therefore the ability to not only advance technological development, but also build proprietary Intellectual Property, pursue near-production development workflows, and actively orchestrate supply and value chains. Crucially, this requires access to manufacturing capacity, EDA infrastructure, and industrial testing environments deeply integrated into the product development cycle.

Open hardware platforms like RISC-V provide streamlined access to chip development. Open-source EDA tools and modern cloud infrastructure are increasingly rendering expensive, proprietary licenses obsolete. The use of independent platforms is strongly favored. Proprietary solutions such as CUDA, which lock teams into single-vendor ecosystems, should be avoided.

Integrating industrial end-users as co-designers, launch partners, and validation partners is another core element of the Challenge setup. Lead customers across sectors like data centers, automotive, logistics, and digital infrastructure will join early in the process to ensure solutions are tuned for real-world deployment. Public procurement initiatives, including those under the EU Chips Act, can generate additional market pull and drive the scale-up of developed technologies.

Demonstrable industry connections are advantageous for the application, though large-scale consortia are not required. Industry partnerships can be expanded step by step

throughout the Challenge. SPRIND and NADI will actively support this process, including hosting dedicated industry workshops to introduce prospective application partners and facilitate connections across the entire value chain.

5. PROCESS

The Challenge is scheduled to run for a total period of about 20 months (for details, see Table 1: Timeline).

Interested teams are invited to submit their application online via the submission form. The application deadline is Monday, November 30, 2026, at 11:00 AM CET. A jury of recognized experts will support the evaluation of the applications and select up to seven teams during a selection meeting in Leipzig on December 14–15, 2026, to advance to Stage 1.

The Challenge is structured into two stages, each with defined milestones. Stage 1 spans eight months, starting on December 16, 2026, and concluding on August 31, 2027. At the end of Stage 1, a jury evaluation will take place for entry into Stage 2. During this session, the jury will assess team progress and select up to three teams to proceed to Stage 2. Stage 2 runs for 12 months and is expected to end on August 31, 2028.

The timeline shown below summarizes the overall projected course of the Challenge. SPRIND reserves the right to adjust dates. Participants will be notified of any relevant schedule changes in a timely manner.

Table 1: Timeline

Date	Event
23.09.2026	Launch
30.11.2026, 11 a.m. (CET)	Application Deadline
14./15.12.2026	Pitch Days, Leipzig
16.12.2026	Start of Stage 1
End of August 2027	Pitch Days for Stage 2, Leipzig
Beginning of September 2027	Start of Stage 2
August 2028	End of Stage 2 and of the Challenge
August 2028	Pitch Days / Jury meeting for Winners, Leipzig

STAGE 1: ARCHITECTURE CONCEPT

Duration: 8 months | Estimated start: mid-December 2026 | Teams: 7 | Funding: €2.6 M each

The goal of Stage 1 is to define and validate a complete chip design and system concept, including clearly defined use cases, a software stack architecture, and simulated proof of performance. Teams will develop an architectural and system design positioned explicitly against state-of-the-art reference systems. Target use cases will be established and benchmarks defined. Using the developed abstraction layer, the chip design will be tested on the selected software stack and verified against the runtime architecture. Energy and performance models will be simulated and disclosed along with uncertainty bands. In addition, teams will formulate a comprehensive concept for the AI-driven design process. This includes identifying appropriate AI methodologies for various design tasks, from architecture search to RTL generation and verification.

STAGE 2: VALIDATED IC (INTEGRATED CIRCUIT)

Duration: 12 months | Teams: 3 | Funding: €7 M each

The goal of this stage is to translate the previously validated architecture into a fully specified, verifiable, and implementation-ready system representation. This enables a consistent mapping of the architecture, execution model, and abstraction layer for the selected software stack, establishing the technical foundation for the physical implementation of the computing platform. Throughout this phase, functional correctness of the overall system will be proven, feasibility for hardware- and platform-specific implementation will be validated, and a solid foundation will be established to ensure a reliable transition into physical design (Tape-out Readiness). The AI systems will be advanced to independently execute increasingly complex tasks. The generation of IP design tasks will be demonstrated, covering components such as memory controllers, DSP modules, or Network-on-Chip structures. The quality of the AI-generated designs will be benchmarked and validated against manual references.

6. HOW DOES MY TEAM BENEFIT?

Across both stages, SPRIND and NADI will make up to €9,600,000 (plus VAT, if applicable) available per team, depending on the financial requirements submitted in their applications. Funding is provided as an individual fixed-price contract based on the cost estimates submitted by each team. The ceiling for funding (plus VAT, if applicable) is set at €2,600,000 per team for Stage 1, and €7,000,000 per team for the potential Stage 2. SPRIND utilizes the European instrument of Pre-Commercial Procurement for this funding mechanism (see Participation Agreement).

To help teams reach their full potential, SPRIND and NADI will offer additional support throughout the entire duration of the Challenge. They will actively assist in facilitating access

to prospective cooperation partners and domain experts. Beyond the conclusion of the Challenge, SPRIND may continue to provide financial backing to participating teams if SPRIND, alongside the jury and external experts, identifies significant breakthrough innovation potential.

Successful applicants are expected to maintain an open, collaborative mindset to foster high-performing teams.

7. WHO IS ELIGIBLE TO APPLY?

Applications are open to teams of all legal forms, including universities, non-university research institutions, established companies, startups, and incubators. Standalone research groups or single research institutions are excluded from applying. Incubators are welcome to forward this Call for Submissions to their networks. A company spin-off is required during the course of the Challenge, and this intent should be clearly reflected in the team's application.

Teams are eligible to apply if they are headquartered in the European Union, the European Free Trade Association (EFTA), or the United Kingdom. Individual team members or collaborative partners may be based outside these regions.

Applicants must ensure that the work submitted for the Challenge is not already funded by other public subsidies, avoiding double funding.

The form “DECLARATION ON RUSSIA SANCTIONS” must be completed and submitted together with the application. Filling out this form is mandatory for participation in this Challenge. Only those applicants who have no ties to Russia within the meaning of this declaration are admitted.

8. HOW DOES THE APPLICATION PROCESS WORK?

Applicants are invited to fill out our online application form to apply for this Challenge:

https://www.sprind.org/en/actions/challenges/submissions/ai-native-chip-design

9. HOW DOES REPORTING WORK?

At the end of each stage, participating teams must compile the essential elements of their development progress into a summary report. The report should detail whether the goals outlined in the initial application have been achieved. In addition, it must outline any intellectual property generated, such as know-how, data, or inventions, and include a list of relevant publications where applicable. The report must be submitted 14 days prior to the end of the respective stage, regardless of whether the team intends to apply for the next stage. Further details regarding the requirements and framework for Stage 2 will be shared with participating teams well in advance of the end of the first stage.

Teams are welcome to reach out to the SPRIND and NADI Challenge team at any time with questions regarding the development of their solution.

10. HOW ARE THE TEAMS SELECTED?

Applications are evaluated based on:

- Their potential to become a disruptive innovation (breakthrough potential)
- The effectiveness and feasibility of the proposed work plan (implementation)
- The team's ability to execute this plan (team)
- Cost-effectiveness of the proposed budget and resource allocation (cost effectiveness)

Table 2 below provides an overview of the criteria used to evaluate teams for admission to the Challenge. The categories Breakthrough Innovation Potential, Implementation, Team, and Cost Efficiency carry equal weight in the evaluation process, with teams assessed relatively/in relation/in comparison to one another. This applies to the selection for Stage 1 as well as for all subsequent stages.

All claims must be supported by scientific data. Where specific data is not yet available, teams are requested to provide an estimate, explicitly designated as such.

Table 2: Evaluation criteria for admission to Stage 1

Breakthrough Potential
Does the proposed approach pursue a radical innovation that goes beyond incremental improvements to existing methods?
Does the solution approach have the potential to actually shorten chip design development time from years to weeks, and is this convincingly justified?
Does the approach strengthen a sovereign, European technology landscape in the chip design ecosystem? Does it rely on independent, open technologies and avoid dependencies on proprietary solutions?
Is the full stack approach (hardware, software, industrial application) credibly addressed, or only a partial aspect?
Does the approach pursue the vision of AI becoming the actual chip designer, or does it only aim for point-specific efficiency improvements to existing design processes?

Does the developed technology—both the chip design and the AI-assisted design process—have potential for further application areas beyond the chosen demonstrator?
Does the approach for chip architecture have the potential to exceed current (and expected by the end of the Challenge) benchmarks for energy efficiency and computational performance in the addressed application field—and how significant is this application field in terms of market size, growth potential, and strategic relevance?
Implementation
Are the work packages and timeline based on realistic assumptions regarding resources, expertise, and technology readiness? Are the planned steps plausible and coordinated?
Is the architecture and system design thoroughly thought through, qualitatively positioned relative to state-of-the-art reference systems, and validated with concrete metrics? Does a coherent software stack concept, including an abstraction layer, exist?
Does a prototype or simulation proof already exist to demonstrate potential feasibility?
Is foundry compatibility considered early on (e.g., access to pilot lines)? Does a plan for the tape-out process and scaling of processes exist?
Are external partners and subcontractors meaningfully integrated?
Is SPRIND funding crucial to driving this breakthrough at maximum speed?
Team
Does the team have the necessary expertise, drive, and innovative strength for the Challenge? Have important gaps in the team structure been identified and a plan presented to recruit missing expertise or enter into partnerships?
Does the team bring diverse perspectives, backgrounds, and experiences to the process? In terms of scientific disciplines, career stages, nationalities, genders? Does the diversity strengthen the team's ability to solve complex challenges?
Is collaboration with ecosystem partners along the value chain planned? Is the team capable of building a renowned network in science, policy, and/or business?
Does the team have practical experience in chip design, setting up AI agentic workloads, or semiconductor manufacturing?

Does the team have relevant experience in building companies in fast-growing startups? Is the team capable of securing follow-up funding during or after the two stages? Does a plan exist to mobilize private venture capital?
Does the proposal clearly state the current legal status of the team (e.g., existing spin-off)? Is there a credible, robust, and realistic roadmap for founding a company by the start of the Challenge or in Stage 1?
Cost Efficiency
Are the requested funds in an appropriate proportion to the intended technological breakthroughs and the scope of work?
Does the budget demonstrate highly efficient use of funds across personnel, hardware, prototyping, and testing?

11. STAGES, MILESTONES, AND STAGE-SPECIFIC EVALUATION

STAGE 1: ARCHITECTURE CONCEPT – DELIVERABLES

- Demonstration of an AI-driven design process for the architecture phase
- Architecture & System Design: Definition of chip architecture and system boundaries, positioning against state-of-the-art reference systems, architectural decisions including rationale
- Use-Case Definition & Benchmarking: Specific industrial target application, definition of benchmarks and comparative metrics, market and application positioning
- Instruction Set Architecture (Conceptual Phase): ISA design at the conceptual level considering Pytorch compatibility, alignment with target workloads, preparation for subsequent RTL implementation
- Software Stack Compatibility: Abstraction layer plus runtime architecture (concept + simulation), AI framework mapping, definition of hardware-software co-design, maturity level: simulation / prototyping, no mandatory implementation
- Simulation & Performance Modeling: Energy and performance models, comparison with relevant state-of-the-art systems, full disclosure of all assumptions and uncertainty bands, sensitivity analysis of key parameters
- Manufacturing & Implementability Analysis: Early assessment of foundry compatibility, packaging options, EDA feasibility, and identification of critical showstoppers

- Interface & Compatibility Concept: Definition of external bus and memory interfaces, proof of compatibility with existing ecosystems (board designs, cooling concepts, power delivery)
- Security-by-Design Concept: Documentation of the security architecture, threat analysis, planned mitigation strategies
- IP Structure: Definition of hardware, software, and architectural IP, ownership and licensing models, commercialization strategy
- Integrated White Paper: Architecture + market + technology + simulation results, including benchmarks and system-level impacts
- Concept for AI-driven Design Process: e.g., RTL generation, HDL debugging, testbench creation, verification

Table 3: Evaluation criteria at the end of Stage 1

Breakthrough Potential
Has the team demonstrated measurable progress against current market standards regarding technological benchmarks for the chip from initial simulations? And regarding the development time of the architecture phase of chip design?
Is the degree of automation of the AI-assisted design process transferable and scalable? Can the quality of AI-generated designs be validated against reference designs?
Does a scalable business model exist that remains viable beyond the Challenge?
Implementation
Have the deliverables of Stage 1 been achieved? If not, why not?
Does a plausible roadmap for physical manufacturing exist?
Do the teams have secured access to manufacturing capacities, EDA infrastructure, and industrial testing environments?
Is the ownership and licensing model clarified?
Team

Does the company have a leadership team that can ensure execution of the next stage? Is the necessary expertise present in the team?
Have missing competencies for Stage 2 been identified and corresponding partners or employees planned?
Does a plan exist to mobilize private venture capital?
Cost Effectiveness
Are the requested funds in an appropriate proportion to the intended technological breakthroughs and the scope of work?
Does the budget demonstrate highly efficient use of funds across personnel, hardware, prototyping, and testing?

STAGE 2: VALIDATED IC – DELIVERABLES

- Demonstration of an AI-driven design process for the logic design phase
- Architecture-Level Implementation: Execution of the computing platform at an appropriate implementation level, e.g., RTL description languages such as Verilog, SystemVerilog, or Chisel for digital architectures, or functional/physics-based modeling methods for alternative computing paradigms, including modular structure and consistent mapping of the architecture to the respective representation level
- Functional Verification: Testbenches + simulations, formal / semi-formal verification of critical modules, proof of correctness against the Stage 1 architecture
- System and Software-Hardware Co-Validation: Validation of target workloads on the respective implementation or simulation environment of the computing platform, including alignment of the compiler and software stack with the hardware and system representation, as well as a consistent end-to-end flow (Software → Architecture Model → Implementation Level → Simulated or Emulated Execution)
- Performance & Power Pre-Estimation: Early, realistic estimation of timing, energy, and throughput, paired with a gap analysis against the Stage 1 simulation
- EDA Tool-Chain Integration: Full integration into industrial design flows, achieving synthesis readiness
- IP Modularization: IP blocks defined, interfaces stabilized, preparation for physical design complete

- Proof of Autonomous IP Generation: e.g., memory controllers, DSPs, Network-on-Chip structures, or AI accelerators
- Quality Validation of AI-Generated Designs against manual reference baselines
- Integration of AI components into the overall design flow

Table 4: Evaluation criteria at the end of Stage 2

Breakthrough Potential
Does the solution approach demonstrably pursue a radical innovation with clear progress against current market standards — especially regarding computational performance, throughput, latency, and performance per watt?
Has a consistent end-to-end flow been realized (software → architectural model → implementation level → simulated execution)?
Has the quality of AI-generated designs been validated against manual references and does it exceed current benchmarks?
Implementation
Has the architecture-near implementation been fully realized, with all IP blocks defined, interfaces stabilized, and preparation for physical design completed?
Have the target workloads been validated on the implementation or simulation environment, and has the alignment of the compiler or software stack with the hardware or system representation been completed?
Has an AI-assisted design process for the logic design phase been demonstrated, and has autonomous IP development been proven (e.g., memory controllers, DSP, network-on-chip)?
Has tape-out readiness been achieved—with validated foundry compatibility?
Have reliable partnerships with lead customers and the entire value chain been established?
Team
Does the team have interdisciplinary expertise for the upcoming tape-out phase?

Is the company structure equipped with an appropriate governance structure?
Does the team have a realistic financing path for the production phase (matching financing, private venture capital)?
Cost Effectiveness
Were the funds used efficiently and in reasonable proportion to the demonstrated results?

12. CONFIDENTIALITY

SPRIND and NADI will treat all submissions confidentially. Information about the submissions will only be shared with the jury, reviewers, and the Challenge coaches. These persons are also obliged to maintain confidentiality.

The selected teams of the Challenge will be announced publicly. By submitting an application, the teams agree to this.

13. WHO CAN I CONTACT FOR FURTHER QUESTIONS?

Applicants are asked to take a look at the participation agreement and the FAQs. Should you not find the answer to your question there, please contact *challenge@sprind.org* for further clarification.

Note: *The process described represents the current state of planning. For any future changes, please refer to the provisions in the participation agreement.*